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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,780	07/21/2003	Atsushi Yusa	OKI.553	4253

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EXAMINER	
LE, DIEU MINH T	

ART UNIT	PAPER NUMBER
2114	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/622,780	YUSA, ATSUSHI	
	Examiner	Art Unit	
	Dieu-Minh Le	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 April 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 August 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Part III DETAILED ACTION

Specification

1. This Office Action is in response to the RCE filed on 04/16/07.

2. Claims 1-25 are presented for examination.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1-16, 18-25 are rejected under 35 U.S.C. 102(e) as being anticipated over Kobayashi et al. (Pub. No. U.S. 2002/0143517t hereafter referred to as Kobayashi).

As per claim 1:

Kobayashi explicitly teaches the invention:

- A circuit for detecting an abnormal operation of memory [abstract, col. 2, par. 0034; col. 4, par. 0058; col. 7, claim 5] comprising:

- a delay circuit for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto [abstract, col. 1, par. 0012; col. 2, par. 0034; col. 4, par. 0058; col. 7, claim 1, col. 8, claim 15];

- a comparison circuit for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other [col. 4, par. 0058 and 0069].

As per claim 2:

Kobayashi further explicitly teaches:

- an access speed of the memory is detected (i.e., ***read/write and storing to and from memory***) [col. 4, par. 0059; col. 6, par. 0097; col. 7; par. 0103].

As per claim 3:

Kobayashi further explicitly teaches:

- a circuit for holding address information in case of noncoincidence in response to the noncoincidence signal [col. 4, par. 0058].

As per claim 4:

Kobayashi further explicitly teaches:

- a circuit for sounding an alarm when the noncoincidence signal is output (i.e., ***abnormal verification***) [col. 2, par. 0034; col. 7, claim 5].

As per claim 5:

Kobayashi further explicitly teaches:

- a circuit for executing an interruption (i.e., ***timing out processes***) when the noncoincidence signal is output [col. 3, par. 0037; col. 6, par. 0090; col. 7, par. 101].

As per claim 6:

Kobayashi further explicitly teaches:

- a delay time of the output data of the memory can be adjusted (i.e., ***delaying calculation, modification***) in the delay circuit [col. 4, par. 0058; col. 5, par. 0083, col. 7; claim 6].

As per claim 7:

Kobayashi further explicitly teaches:

- memory is a flash memory (i.e., ***a recorded medium, a programmable medium, a portable recorded medium***) [col. 7, par. 103].

This is clearly shown that Kobayashi's computer system malfunction/abnormal having failure/error detection and correction capability via delay circuit means are corresponding to Applicant's invention.

As per claims 8 and 18:

Due to the similarity of claims 8 and 18 to claims 1 and 3 except for an integrated circuit comprising a memory, delaying circuit, and comparison circuit etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of a delay circuit for delaying an output data, a comparison circuit for outputting a noncoincidence signal, etc…; therefore, this claim is also rejected under the same rationale applied against claims 1 and 3. **In addition, all of the limitations have been noted in the rejection as per claims 1 and 3.** Such as an integrated circuit comprising a circuit for detecting an abnormal operation of computing system is clearly

disclosed by Kobayashi (i.e., ***semiconductor memory device***) [abstract, col. 7, claim 1].

As per claims 9-16:

Due to the similarity of claims 9-16 to claims 1-7 except for a method for detecting an abnormal operation of memory comprising delaying and output step, outputting an incoincidence signal step, comparison step, etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of a delay circuit for delaying an output data, a comparison circuit for outputting a noncoincidence signal, etc…; therefore, these claims are also rejected under the same rationale applied against claims 1-7. **In addition, all of the limitations have been noted in the rejection as per claims** 1-7.

As per claims 19-25:

Due to the similarity of claims 19-25 to claims 1-7 except for an integrated circuit comprising a memory, a delaying circuit, a comparison circuit, etc… instead of a circuit for detecting an abnormal operation of memory comprising capabilities of a delay circuit for delaying an output data, a comparison circuit for outputting a noncoincidence signal, etc…; therefore, these claims are also rejected under the same

rationale applied against claims 1-7. **In addition, all of the limitations have been noted in the rejection as per claims** 1-7.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi et al. (Pub. No. U.S. 2002/0143517t hereafter referred to as Kobayashi) in view of Fujiwara et al. (U.S. Patent 5,640,508 hereafter referred to as Fujiwara).

As per claim 17:

Kobayashi explicitly teaches:

- A circuit for detecting an abnormal operation of memory [abstract, col. 2, par. 0034; col. 4, par. 0058; col. 7, claim 5] comprising:

- a delay circuit for delaying an output data output from the memory for a predetermined period of time and for outputting a delayed data responsive thereto [abstract, col. 1, par. 0012; col. 2, par. 0034; col. 4, par. 0058; col. 7, claim 1, col. 8, claim 15];

- a comparison circuit for outputting a noncoincidence signal when the output data output from the memory and the delayed data are not coincident with each other [col. 4, par. 0058 and 0069].

Kobayashi does not explicitly teaches:

- a first and second latches circuits for stores output data and the delayed data.

However, Kobayashi does disclose capability of:

- A computer system malfunction/abnormal having failure/error detection and correction capability via delay circuit means [col. 5, lines 8-25].

- an integrated circuit comprising a circuit for detecting an abnormal operation of computing system (i.e., ***semiconductor memory device***) [abstract, col. 7, claim 1].

In addition, Fujiwara does explicitly disclose:

- A fault detection and correction system having latches circuits [abstract, col. 1. lines 30 through col. 2, lines 55 and col. 7, claim 4] comprising:
- ***multi-latches circuits used in supporting error detection/correction and data comparison process via delay circuitry*** [col. 1. lines 30 through col. 2, lines 55 and col. 7, claim 4].

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to realize that the combination of Kobayashi's ***computer system malfunction/abnormal having failure/error detection and correction capability via delay circuit means*** and Fujiwara's ***multi-latches circuits used in supporting error detection/correction and data comparison process via delay circuitry*** do perform such Applicant's first and second latches circuits for stores output data and the delayed data limitation. This is because Kobayashi and Fujiwara clearly applied these

circuitries for testing configuration, comparison, storing, simulation, evaluation, performance in determining whether the system functioned properly; second, by utilizing this approach, the computer memory data processing system, more specifically an memory abnormal operation detection system can enhance its operation performance, more specifically to ensuring the error thoroughly detected and corrected via the delaying and comparison processes.

This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so to improve the computer memory data system operation availability and network/system performance therein with a mechanism to enhance the data connectivity, data debugging, data displaying, data reliability, and data throughput which eventually will increase its performance, such as data throughput between internal and external devices.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. A shortened statutory period for response to this action is set to expired THREE (3) months, ZERO days from the date of this

letter. Failure to respond within the period for response will cause the application to be abandoned. 35 U.S.C. 133.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (703)305-9408. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 6:30 PM.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dieu-Minh Le whose telephone number is (571) 272-3660. The examiner can normally be reached on Monday - Thursday from 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571)272-3644. The Tech Center 2100 phone number is (571) 272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DIEU-MINH THAI LE
PRIMARY EXAMINER
ART UNIT 2114

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06/10/07